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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,718	03/04/2002	Hirokazu Miyagawa	H-1031	2190

7590 04/23/2003

MATTINGLY, STANGER & MALUR
ATTORNEYS AT LAW
1800 DIAGONAL ROAD, SUITE 370
ALEXANDRIA, VA 22314

EXAMINER

NGUYEN, VINCENT Q

ART UNIT PAPER NUMBER

2858

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

10/086,718

Applicant(s)

MIYAGAWA ET AL.

Examiner

Vincent Q Nguyen

Art Unit

2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Pre-Amendment filed March 04, 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 10 is/are rejected.
- 7) ☒ Claim(s) 7-9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Objections

1. The examiner is confusing because claims 2 recites said phase comparison circuit, and said control voltage generation circuit forming in unison a phase-locked loop (Lines 11-12) whereas, claim 3 recites a path separate from the path of said phase locked loop. How come the path is separated? Appropriate correction and/or explanation is required. For the purpose of examination, the Examiner assumes that any path would be considered as a path separate from the path of the phase locked loop.

Claim 10 recites the limitation "wherein said method" in the first line of the last paragraph. There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination, the examiner assumes it is a "step of activation". In addition, the method recites in claim 10 is unclear since it does not contain any step to perform the testing the oscillation circuit but recites elements similar to the device recited in claim 1. For the purpose of examination, the examiner assumes the method is read out from the apparatus of claim 1.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 5, 6, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaplik et al. (5,412,353).

Regarding claims 1, 6, 10, Chaplik et al. discloses a device (figure 2) which controls a voltage-controlled oscillation circuit (10) with a first control voltage (62) to produce a base frequency signal, controls the voltage-controlled oscillation circuit (10) with a second control voltage (70) which is derived from data (60) to be transmitted thereby to implement the frequency modulation, and implements the data transmission by changing (48) the base frequency, wherein a circuit (44) of producing the second control voltage (70), the variation of the second control voltage (70) of the voltage-controlled oscillation circuit (40) in response to the change of base frequency exhibits a characteristic that is opposite (See figure 3a-3f) to the characteristic of modulation frequency deviation of the voltage-controlled oscillation circuit (40). The only difference between Chaplik and the invention claimed is that the claim recites the circuit (44, 46) has its reference current value controlled in response to the change of the base frequency while Chaplik does not explicitly disclose. However, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to recognize that in order for the oscillator to be controlled, the voltage controlled oscillator (VCO) must increase or decrease the voltage or current to lock the oscillator oscillating at a desired frequency. Thus, the signal 66 must have reference current so that the loop filter (46) and the adjuster (48) would adjust the phase error (See MPEP 2144.03).

Regarding claim 2, Chaplik discloses a phase comparison circuit (44) which compares in phase the oscillation output (60) of said voltage controlled oscillation circuit

(40) with a reference clock signal (66), and a control voltage generation circuit (46, 48) which generates, in accordance with the phase difference detected by said phase comparison circuit, such a voltage that the phase difference ($\Delta\omega$) dissolves and applies as the first control voltage (62) to said voltage-controlled oscillation circuit (40), said voltage controlled oscillation circuit (40), said phase comparison circuit (44), and said control voltage generation circuit (46, 48) forming in unison a phase-locked loop.

Regarding claim 3, Chaplik discloses said second control voltage (70) is supplied to said voltage-controlled oscillation circuit (40) through a path separate from the path of said phase-locked loop.

Regarding claim 5, Chaplik et al. does not disclose a variable counter circuit (Column 4, lines 30-37) which counts the oscillation output of said oscillation circuit, and a register (Column 36, lines 35-40) which sets a value to be counted by said variable counter circuit, the base frequency being changed in response to the alteration of the value set in said register, the reference current value being controlled in accordance with the value set in said register (See also figure 18).

4. Claims 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaplik et al. (5,412,353) in view of Zuta et al. (6,016,080).

Regarding claim 4, Chaplik does not disclose a digital filter. Zuta et al. discloses a system similar to that of Chaplik and further disclose (Figure 19) a digital filter (785) which samples a digital transmission data signal (786) and implements a computation for the sampled signal, and a D/A conversion circuit (78) which implements the D/A

conversion for the output of said digital filter (785), said controlled reference current value being the reference current value of said D/A conversion circuit (See column 35, lines 22-40). It would have been obvious to one of ordinary skilled in the art at the time the invention was made to recognize the desirability of modifying Chaplik et al. to incorporate the digital filter as taught by Zuta et al. into the system of Chaplik because it would have been desirable to increase the efficiency of the implementation of the VCO (See Zuta et al.'s column 37, lines 49-54).

Allowable Subject Matter

5. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Q Nguyen whose telephone number is (703) 308-6186. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

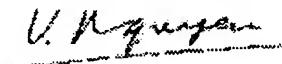
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (703) 308-0750. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-5841 for regular communications and (703) 308-5841 for After Final communications.

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Art Unit: 2858

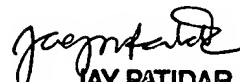
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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vincent Q. Nguyen



April 18, 2003



JAY PATIDAR
PRIMARY EXAMINER